Technical Abstracts

In Case You Missed It…

Starting this month, CIRCUITS ASSEMBLY will provide abstracts of papers from recent industry conferences. Our goal is to provide an added opportunity for readers to keep abreast of technology and business trends. This month's abstracts come from papers presented at SMTA International, September 2004; for the full papers, contact smta.org.

Packaging

"Camera Module Packaging Technology"

Authors: Robert Darveaux, Asif Chowdhury, Jay Tome, Ron Schoonejongen, Mitch Reifel, Archie De Guzman and Sung Soon Park, all of Amkor Technology; rdarv@amkor.com.

Abstract: Packaging an image sensor in a camera module presents several unique engineering challenges. Materials selection, assembly process, optical test and facilities control are all areas where technology is rapidly developing. This paper focuses on current challenges, and highlights several areas where advances in R&D are needed.

"Qualification and Reliability for MEMS and IC Packages"

Author: Reza Ghaffarian, Ph.D., Jet Propulsion Laboratory; reza.ghaffarian@jpl.nasa.gov.

Abstract: Advanced IC packages are moving toward miniaturization from two key different approaches, front- and back-end processes, each with their own challenges. Direct flip-chip die is the most efficient approach when the issues of known good die and board/assembly are resolved. WLP packages solve the issue of known good die by enabling package test, but have limitations (I/O limits, costs, reliability). From the back-end approach, system-in-package (SiP) is developing due to an increasing demand for package and die integration of different functions into one unit to reduce size and cost and improve functionality. MEMS add another challenge since they include moving mechanical elements. Conventional qualification and reliability need to be modified and expanded in most cases to detect new unknown failures. This paper reviews four standards released or being developed that address qualification and reliability of assembled packages. It presents mechanical and thermal cycle qualification data generated for a MEMS accelerometer.

Process Control

"Process Window Study Determining the Defect-Free Processing Window For Small Surface-Mount Components Using a Response Surface Design of Experiment"

Author: Michael Johnston, Micron Technology; msjohnston@micron.com.

Abstract: The integration of smaller surface-mount devices requires tighter, more capable manufacturing procedures for screen printing and placement. This paper reports results of a design of experiment (DoE) used to determine the process window for a typical 0402x4 resistor network. The factors of the DoE include solder paste alignment and part placement in the x and y directions. The result of the process window DoE determined the placement of a 0402x4 resistor network to be a circle, centered at the CAD location with a diameter of 0.002" to attain a process capability index (Cpk) of 1.50.

Soldering

"An Obstacle-Controlled Creep Model for Sn-Pb And Sn-Based Lead-Free Solders"

Author: Jean-Paul Clech, EPSI Inc.; jpclech@aol.com.

Abstract: This paper presents the application of physically-based, obstacle-controlled creep models to the analysis of steady-state creep rates for eutectic SnPb and seven lead-free solders: Sn58Bi, Sn0.7Cu, Sn3.5Ag, Sn4Ag, Sn3.8Ag0.7Cu, Sn3.5Ag0.75Cu and Sn2.5Ag0.8 Cu0.5Sb. For each alloy, one set of steady-state creep measurements is used to determine scaling constants and physical parameters of the model (four or eight constants in total for the one- or two-cell models, respectively). Each model is then tested against independent test results (as many as nine test cases for the Sn3.5Ag alloy). The obstacle-controlled, solder creep models permit the bridging of tension, compression and shear test results as well as creep, strength and stress relaxation data, often without – and sometimes with – the use of a simple, multiplicative calibration factor. The models also permit the prediction of solder joint stress/strain measurements during thermal cycling of soldered assemblies. The need for calibration factors suggests that creep models derived from a given mechanical test, and specimen type or size, should not be used without justification in the stress/strain analysis of soldered assemblies. Model calibration and validation is a critical step in the application of creep models to stress analysis or reliability models. The use of obstacle-controlled creep models resolves many anomalies observed in the classical analysis of lead-free solder creep data, including activation energies and power-law exponents that were found to be stress- and/or temperature-dependent.

"0.8 mm BGA Solder Joint Reliability Under Flexural Load"

Authors: Phil Geng, Alan McAllister, Carolyn McCormick, Mitul Modi and Arnaldo Nazario, all of Intel Corp.; phil.geng@alum.mit.edu.

Abstract: This work investigated 0.8 mm flip chip BGA solder joint strength under bending load. The DoE included eutectic lead and SnAgCu materials, solder resist openings, solder ball diameters, metal-defined and soldermask-defined pads. Results showed that solder joint strength of SnAgCu solder is lower than that of traditional SnPb solder. With the specific fourpoint bend setup at high speed loading, the bend test results implied that the SnAgCu solder joint under shock load can result in more brittle failure. SnAgCu solder joints showed more package-side failures. ■

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