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本文讨论倒装芯片的底部填充工艺以至无铅助焊剂残留。助焊剂与底部填充的相互作用对于底部填充倒装芯片设备的长期可靠性很重要。所有的助焊剂在回流后都会形成残留。经过适当处理后，免清洗或低残留助焊剂的残留不会降低电气性能，但会影响底部填充的粘合以及流动。增高的无铅加工温度会在回流后改变助焊剂残留的特性。本研究探讨粘性助焊剂在无铅倒装芯片回流过程中提供可靠稳定的相互连接的能力。

Flip Chip Underfill and Flux Residue with Lead Free

Brian J. Toleno, Ph.D., and George Carson, Ph.D.

This study presents data on the compatibility of 17 different flux systems with two underfill systems in a lead-free flip chip assembly process.

Worldwide, electronics manufacturers are investigating new lead-free alloys and their effects on the reflow process, an important first step in developing robust lead-free processes. Once lead-free processes are well developed, determining the effect of these changes on the various materials sets used in electronic assemblies is important.

The leading lead-free alloy candidates are the different tin-silver-copper (Sn/Ag/Cu) formulations (often abbreviated as SAC) recommended by NEMI¹ in the U.S. and IRTI in the European Union.² The Sn/Ag/Cu eutectic system has a melting point of 217°C, significantly higher than the 183°C melting point of eutectic tin/lead (Sn/Pb) alloy. These new alloys increase the peak reflow temperature from 220°C up to 240 or 260°C, a factor that affects material performance. This study deals with one aspect of lead-free processing for flip chip in a package: flip-chip underfill adhesion to lead-free flux residues.

The interaction between the flux and the underfill is important for the long-term reliability of underfilled flip chip devices.^{3,4} All fluxes leave behind residues after reflow. When properly processed, no-clean or low-solid flux residues do

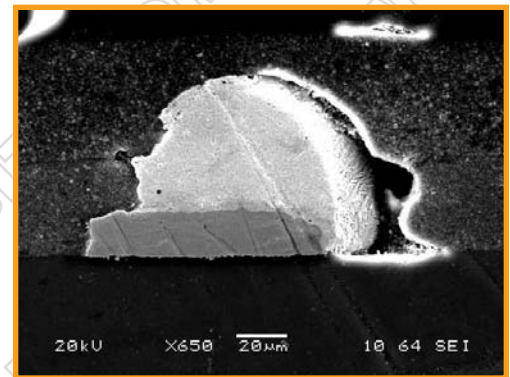
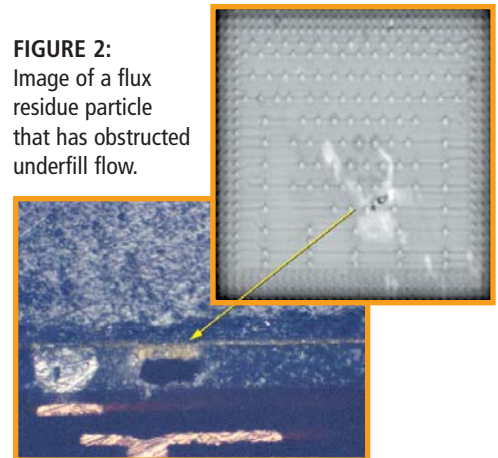


FIGURE 1: SEM micrograph of voiding due to flux residues.

FIGURE 2: Image of a flux residue particle that has obstructed underfill flow.



not degrade electrical performance (such as with SIR and ECM) but will affect the adhesion and flow of the underfill. Elevated lead-free processing temperatures change the characteristics of the flux residues after reflow.

This study examines tacky fluxes for their ability to provide a reliable and consistent interconnect in a lead-free flip chip reflow process. After initial evaluation, parts were conditioned, and

reliability was assessed to determine JEDEC level 3 with a 260°C reflow compatibility. The 260°C peak reflow temperature simulates the worst possible reflow conditions that a package can undergo in a surface-mount manufacturing process. Parts were then evaluated using scanning acoustic microscopy for evidence that the flux residues affected reliability (Figure 1).

Flux residues can affect reliability in two different ways. Present on the solder bump, substrate or die, thin films of flux residue can significantly reduce interfacial adhesion between the flux and the surfaces. Once the underfilled device is stressed by thermal shock, humidity or other factors, the underfill delaminates from the surface, and a gap can be detected using acoustic microscopy.

Fluxes can also affect reliability by physically impeding the flow of underfill material. Flux residue buildup in the gap between bumps or between the die and the substrate can narrow the gap to a point where the underfill cannot flow (Figure 2), or the edges flow faster, encapsulating air and creating a void.

To ensure a void-free underfill, homogeneous wetting of the underfill must occur on all surfaces. If wetting is not homoge-

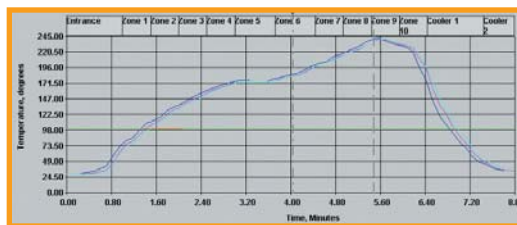


FIGURE 3: Lead-free profile used to reflow test vehicle.

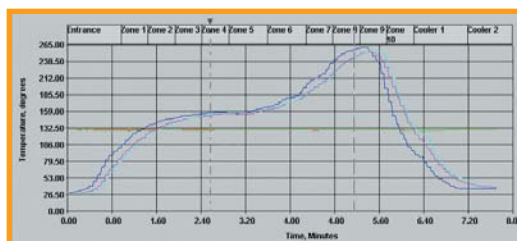


FIGURE 4: Reflow profile used for JEDEC moisture resistance testing (260°C peak temperature).

nous, voids in the uncured underfill may translate into reliability problems later.

With the change to a lead-free reflow process, the characteristics of the flux residues change significantly. This study presents data and analysis on the compatibility of 17 different flux systems with two underfill systems in a lead-free flip chip assembly process.

Experimental

The test component was a 14.4 x 14.4 mm flip chip with polyimide passivation. The bump pattern was a full array of 3,840 bumps at a pitch of 225 µm. Two

Property	UF A	UF B
Curative	Anhydride	Anhydride
Filler	42% (silica)	64% (silica)
CTE (α_1)	44	22
T _g	140	120

TABLE 1: Underfill systems used in lead-free flux evaluation.

Level	Time	Conditions
1	168	85°C / 85%RH
2	168	85°C / 60% RH
2a	696	30°C / 60% RH
3	192	30°C / 60% RH
4	96	30°C / 60% RH
5	72	30°C / 60% RH
5a	48	30°C / 60% RH
6	TOL	30°C / 60% RH

TABLE 2: JEDEC pre-conditioning environment as per J-STD 022A.

lead-free alloys were used as bump metallurgy: Sn/3.5 Ag/0.5 Cu and Sn/3.0 Ag/1.0 Cu. The substrate was a four-layer BT laminate at a thickness of 1 mm. The solder mask was PSR4000 AUS5, and the surface finish on the pads was electroless nickel/immersion gold (ENIG).

The assembly was performed using the following procedure. The flip chips were dipped into a flux pot with a dip/coating height set to 50 microns and placed using an SEC Model 850. The parts were then reflowed using a BTU Paragon 150, under nitrogen (less than 30 ppm O₂) using a lead-free profile with a peak temp of 245°C (Figure 3). After reflow, the devices were underfilled with either of two underfills (Table 1) using an Asymtek C270 automated dispenser. Both underfills were treated to the same cure cycle: ramp to 165°C over one hour, then held at 165°C for one hour.

After curing, a Sonoscan D6000 scanning acoustic microscope imaged all parts using a 100 MHz transducer (time 0 scans). At this point, some parts were set aside for cross-sectioning to measure the die to substrate gap.

After recording the initial acoustic images, the parts were conditioned as per JEDEC level 3 testing (Table 2). Parts were baked at 125°C for 24 hours to establish the same moisture level baseline for all parts, then conditioned for 192 hours at 30°C/60% relative humidity (RH), as per the J-STD-022. After conditioning, the

Flux	Run 1		Run 2		Run 3	
	Underfill Gap (µm)	Joint Quality	Underfill Gap (µm)	Joint Quality	Underfill Gap (µm)	Joint Quality
A					60	Good
B	70	Good	77	Good	63	Good
C	73	Good	83	Good	64	Good
D			91	Excess Flow		
E			83	Good	60	Good
F	77	Fair	102	No Connection	108	No Connection
G	76	Fair	81	Good	62	Good
H	66	Good	81	Good		
I	86	Poor				
J			83	Good	63	Good
K					65	Good
L			80		63	Good
M			81	Good	65	Good
N			83	Good	64	Good
O			83	Good		
P					61	Good
Q	77	Fair	84	Good		

TABLE 3: Initial solder joint evaluation.

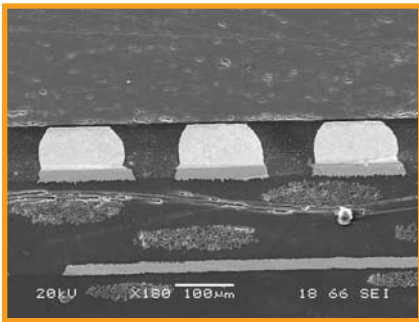


FIGURE 5: Cross section picture of a good solder joint, Flux K.

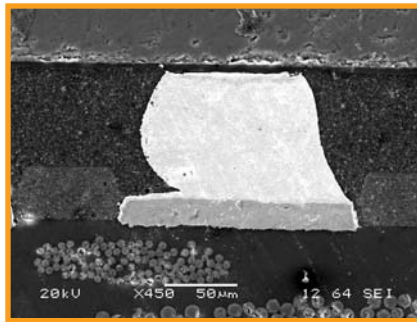


FIGURE 6: Cross section picture of a poor solder joint, Flux I.

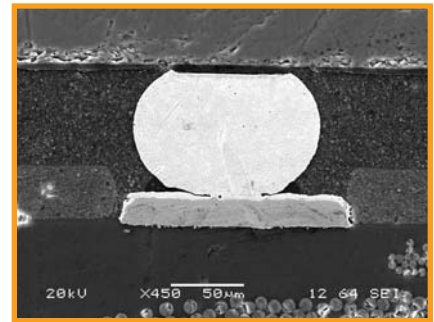


FIGURE 7: Cross section picture of an open with Flux F.

parts were subjected to three lead-free reflows with a peak temperature of 260°C (Figure 4) and imaged again using the acoustic microscope.

Results

Initial Wetting

Wetting and gap height were measured on select samples. When the flux system worked properly, the solder bump melted and wetted out along the pad, the package collapsed, and the overall gap height was reduced. Based on gap heights, fluxes were designated with performances of good, fair or failure. Failures correspond to a lack of connection between the flip chip and the substrate pads. A summary of the results is presented in Table 3.

Solder joints were evaluated over three separate builds. Since slight variations occurred in the solder mask definition, the gap heights were only comparable within a column. Other criteria used to evaluate soldering performance were wetting to the pad, bump shape after collapse and overall solder joint appearance.

Most fluxes met the requirements of lead-free reflow of flip chips in a nitrogen environment. Figure 5 shows a good solder joint with good wetting along the pad and a collapsed bump. Figure 6 illustrates a fair solder joint with poor wetting to the pad. The worst performer did not form a solder connection at all—when the part was underfilled and cured, the device floated (Figure 7).

All parts, except the ones assembled with the flux that did

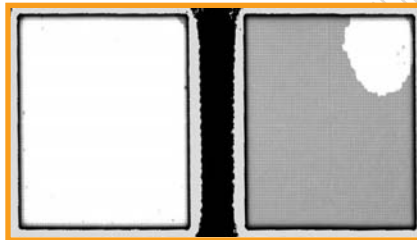


FIGURE 8: Acoustic microscope image of a popcorn void present after reflow, Flux B and Underfill A.

not allow reflow, were placed into the next segment of the testing.

JEDEC Level 3/260°C Reliability

This study used JEDEC testing to determine flux residue/underfill compatibility. With flux residue compatibility, moisture conditioning and subsequent thermal treatment can force a failure when moisture intrudes where the underfill does not adhere well to the flux residue. As flux residues may be slightly hygroscopic, any moisture that does pen-



FIGURE 9: An example of acoustic microscope images of a flux (Flux D) incompatible with both underfill systems, Underfill B on the top row and Underfill A on the bottom.

etrate an exposed flux surface can be absorbed. This condition is exacerbated when poor adhesion occurs between the underfill and the flux residues.

After exposure to moisture conditioning, the parts were reflowed three times with a peak temp of 260°C. During reflow, any absorbed moisture within the part expands (popcorning), creating the voids observed in the acoustic microscopy images (Figure 8). A summary of all the flux/underfill systems examined and their performance are presented in Table 4. Out of all the fluxes examined, only two were incompatible with both underfill systems (Figure 9). Four fluxes exhibited excellent performance characteristics with both

Flux	Joint Quality	Performance with UF A	Performance with UF B	Overall Performance
A	Good	Good	Fair	UF A only
B	Good	Poor	Good	UF B only
C	Good	Poor	Good	UF B only
D	Poor	Poor	Poor	Poor
E	Good	Fair	Good	UF B only
G	Good	Good	Good	Excellent
H	Good	Poor	Poor	Poor
I	Poor	Poor	Good	UF B only
J	Good	Poor	Good	UF B only
K	Good	Poor	Good	UF B only
L	Good	Good	Good	Excellent
M	Good	Poor	Good	UF B only
N	Good	Good	Good	Excellent
O	Good	Poor	Good	UF B only
P	Good	Good	Good	Excellent
Q	Good	Fair	Good	UF B only

TABLE 4: Summary of flux/underfill performance.

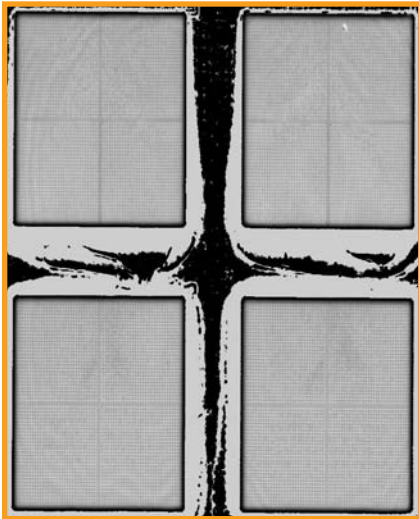


FIGURE 10: Example of acoustic microscope images of a flux (Flux P) that has excellent compatibility with both underfill systems; all images have Underfill B on the top two devices and Underfill A on the bottom two devices.

underfills (Figure 10). Most of the fluxes were compatible only with Underfill System B. One proprietary epoxy flux system showed better performance with Underfill A over Underfill B.

Conclusions

This study evaluated a number of material sets for lead-free processes. The tacky flux and underfill systems are designed for the flip chip packaging process. The movement to a lead-free process affects the moisture level rating of packages and devices.⁵ One of the materials that impacts this JEDEC moisture level rating is the underfill.

This study shows that some flux residue/underfill systems are suitable for lead-free processes. Flux Systems G, L, N, and P are more compatible to different underfill material sets than others. Underfill System B, developed with a chemistry specifically designed to interact with flux residues⁶ and meet JEDEC level 3/260°C requirements, shows excellent compatibility with almost all the flux residues. ■

References

1. C. Handwerker, "NEMI Pb-free Solder Project," *Proc. Technical Program SMTA International*, 2003.
2. www.npl.co.uk/ei/news/pbfree.html.

3. G. Carson and M.E. Edwards, "Factors Affecting Voiding in Underfilled Flip Chip Assemblies," *Proc. Technical Program, SMTA International*, 2001.
4. P.N. Houston, et al., "Low Cost Flip Chip Processing and Reliability of Fast-Flow, Snap-Cure Underfills," *Proc. Technical Program, ECTC*, 1999.
5. M. Kwoka and G. O'Brien, "Pb-free skunk works project," *IPC APEX*, 2000.
6. Flux chemistry and compatibility presented at SMTA International, September 2004.

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