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应在生产线的哪一点上装置AOI自动光学检查——焊膏印刷后、元件贴装后还是焊接后？一些人认为，大部分瑕疵是由使用焊膏造成的，所以最好在这个步骤后测试。其他人则确信，在焊接后进行AOI是发现所有瑕疵的唯一方法。为了获得关于各个加工步骤的瑕疵率以及瑕疵在整个生产过程中性质的信息，在大规模批量生产中进行了全面测试。生产线在焊膏印刷、元件贴装和再流焊后装有AOI系统。本文讨论令人惊讶的测试结果。

AOI Testing Positions in Comparison

Peter Krippner and Detlef Beer

An extensive study compares AOI following printing, placement and reflow, with surprising results.

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When automated optical inspection (AOI) systems are used in the production process for electronic components, the question arises: At which point in the line does AOI make the most sense—following the printing of solder paste, after component placement or after soldering? The opinions differ. On one hand, some think that the majority of faults result from the solder paste application so that testing is best after this step in the process. Others are convinced that AOI following soldering is the only way to find all of the faults. In any case, positioning of the AOI system is of great significance for the process quality and efficiency of the line.

To obtain information on the fault quotas resulting from the individual process steps and how faults behave in the complete production process, a comprehensive test setup was made in large-scale mass production. The line was equipped with modern production equipment, including an AOI system after paste print, component placement and reflow. The systems were set up for a zero-fault strategy. Automatic testing of all relevant test items (paste, components and soldering) was accomplished over a period of one week.

All totalled, 2,500 assemblies marked with barcodes were tested. One printed circuit board (PCB) had 2,274 solder joints so that a total of about 5.7 million solder joints were tested. The pad surfaces consisted of a nickel/gold (NiAg) alloy.

Objective of Test Setup

The test setup was intended to provide information on the following aspects: change in faults during the individual process steps; distribution of the types of faults in the production process and information on the most effective location for the AOI system.

Description of Testing Process

All of the AOI systems in this study operated with the same basic software so that images and fault data from each circuit board could be stored for tracing back and comparison. A specially developed software tool presented a comparative analysis of the results and provided confirmation of the primary causes of faults as well as analysis of the fault focal points.

Every circuit board was tested at all three AOI systems, and the results were transferred to a repair station in each case. There, faults detected were acknowledged and assigned to a fault class. The acknowledgments were stored and relayed to an evaluation station via the network. All results could be classified clearly with a barcode and extension indicating the testing station in question.

Circuit boards with clearly evident faults were not sorted out or repaired. They were allowed to run through the complete production process. This practice, in particular, made following the changes in the individual faults during the process possible.

The production equipment was thoroughly prepared before the test—the template printers,

component placer and reflow oven were serviced and checked. The production personnel were informed and included in the test run.

Fault Coverage

Table 1 shows the faults detected by the paste test, during component inspection and during the post-reflow inspection. Figure 1 provides examples of typical faults that occur during production—specifically, erroneous paste application. (For examples of typical faults that occur during production with component and soldering errors, access the full article at www.circuitsassembly.com/online/0404/0404viscom.shtml)

Paste Inspection	Component Placement Inspection	Post Reflow Inspection
Misplaced paste print		
Print too big		
Smudged print	*if not covered from component*	
Paste bridges	Paste bridges	Short
Incomplete paste print	*if not covered from component*	Thin solder joint
No wetting	No wetting	Open solder joint
Contamination	*if not covered from component*	Contamination
Miscellaneous	Miscellaneous	Miscellaneous
	Missing component	Missing component
	Misplaced component	Component misplacement
	Billboard	Billboard
	Face down	Face down
	Doubled component	Doubled component
	Component wrong coplanarity	Component wrong coplanarity
	Faulty component	Faulty component
		Lifted lead
		Tombstone
		Component not to be soldered

TABLE 1: Types of faults detected by the paste test.

Changes in Fault Types

In analyzing all faults that occurred, fault chains were first made up. The stored fault patterns for all three process steps were cut out for each fault, which indicated the necessity of differentiating between process faults and true faults.

Although process faults produce a clear fault during paste application or installation of components, they do not lead to a true fault following soldering, such as incorrect initial paste application. True faults represent clear faults that require correction following soldering according to IPC 610.

Development of Process Faults

The following fault chains in Figure 2 indicate development of process faults during production. From left to right, the figure shows images following paste printing, after component placement and after soldering. In the image chain itself, green equals fault-free, yellow equals process faults and red equals true faults. (For more fault chains developed during production, please access the full article at www.circuitsassembly.com/online/0404/0404viscom.shtml)

Image Chain 1-3: Twisted or offset components can move to the correct position after soldering. Moreover, this correction possibility in the soldering furnace depends on the weight of the components and their contacting pin surface.

Image Chain 4-5: Application of less paste still leads to a good solder joint following soldering. Generally, a pad on which only 50% of the required paste was present still offered sufficient soldering quality. Certainly, this value could be reduced even more for HAL (hot air level) circuit boards because preliminary tinning is frequently sufficient.

Development of True Faults

The image chains in Figure 3 show the change in true faults during the process. From left to right, the figure shows images

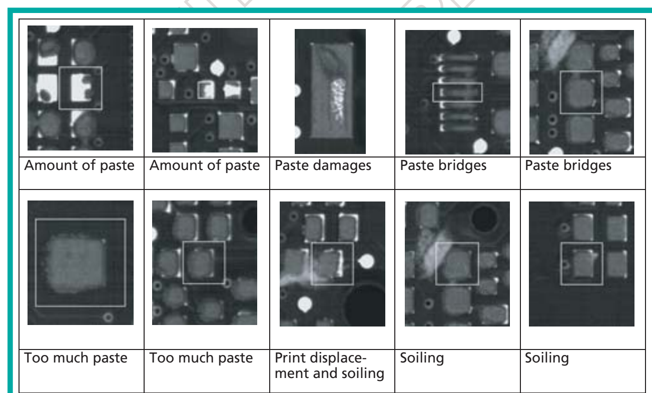

FIGURE 1: Examples of erroneous paste application.

Image Chain	Name	Paste Printing	Component Placement	Soldering
1	Component offset			
2	Component offset			
3	Component twisted			
4	Amount of paste			
5	Amount of paste			

FIGURE 2: Fault chains developed during production.

following paste printing, after component placement and after soldering. (For more image chains showing the change in true faults during the process, please access the full article at www.circuitsassembly.com/online/0404/0404viscom.shtml)

Image Chain 1-6: The image chains show typical assembly faults like wrongly placed or lost components.

Image Chain 7: Mechanically defective components can be recognized after installation or after soldering. Here, a defective component cap can be recognized.

Image Chain 8: As can be seen on the paste print, first, the component was incorrectly placed on the paste and then became lost.

Image Chain 9-10: Diodes installed that were turned the wrong way do not change their position in contrast to light chips. Interestingly, one can recognize the correct pin imprint in the middle image after component installation and that the component was twisted when set down.

Image Chain 11-14: Contamination on the circuit board frequently leads to subsequent faults such as a deposit of paste below the templates and, in this example, to a component placement fault.

The image chains from the test setup are very interesting in themselves, showing the individual steps in the production process. However, they show how difficult evaluating and classifying process faults and true faults directly following the specific process step can be. The final results can only be seen after soldering, and, therefore, only then can one make a reliable statement regarding the quality of the circuit board.

For paste printing, a ratio of 2.5 process faults to each true fault was established; during component placement, one process fault occurred for every true fault. The distribution of process faults within production was particularly interesting. They occurred with stochastic distribution and provided no indication of subsequent true faults. However, fault focal points, such as on certain pads and construction shapes, were noted over the entire time.

Fault Distribution

Of the 2,500 circuit boards, 2,404 were included in the final evaluation. With the remaining 96, clearly categorizing the results on the basis of the barcode was not possible. Of the 2,404 circuit boards, 167 contained faults—the first pass yield (FPY) was 93.1%.

On the 167 circuit boards, 189 single or component faults were present. The fault distribution is shown in Figure 4. For simplification, the following individual faults have been categorized into six fault groups: component faults (component not wettable); component placement faults (component missing, incorrect component position, too many components); contamination; erroneous solder paste printing (too little, missing or smeared paste, bridges); erroneous soldering process (tombstones, lifted leads, bridges); and other.

First pass yield

Figures 5-7 show the FPY and the distribution of true faults and process faults.

Image Chain	Name	Paste Printing	Component Placement	Soldering
1	Component assembly error			
2	Component on edge			
3	Component position incorrect			
4	Too many components			
5	Too many components			
6	Tombstone			
7	Component damaged			
8	Component missing			
9	Component position incorrect			
10	Component position incorrect			
11	Component miscellaneous			
12	Soiling			
13	Soiling			
14	Soiling			

FIGURE 3: Image chains showing the change in true faults during the process.

Fault distribution following individual process steps

During the further process, the fault coverage following the individual process steps was analyzed. The total consisted of 2,404 circuit boards.

After paste print, 14 circuit boards had two true faults and 36 process faults. The FPY following this process step was 97.9%. The number of paste faults in relation to the total number of faults was 8.3% (Figures 5 and 8).

After component placement, 62 erroneous circuit boards and 65 with process errors were detected. The 62 erroneous circuit boards also included the 14 erroneous paste boards. The circuit boards with process faults could only be recognized to a limited extent. The FPY following this process step was 94.7%. The number of faults after component placement in comparison to the total number of faults was 46% (Figures 6 and 8).

Post reflow, the AOI was used as a reference system. The FPY was 93.1%, or 6.9% true faults on 2,404 circuit boards. The highest number of defects was detected after the soldering process. Additionally, to the faults detected after paste printing and assembly, the soldering defects can be detected here, too. The percentage of detected defects after the soldering process was 99.5% (Figures 7 and 8).

After soldering and AOI testing, the circuit boards were subjected to an in-circuit test (ICT). Fifty-two percent of the recognized AOI faults were recognized by ICT. ICT was not capable of detecting missing block capacitors or chip resistors with lifted leads (for example, Image Chain 13 in Figure 3).

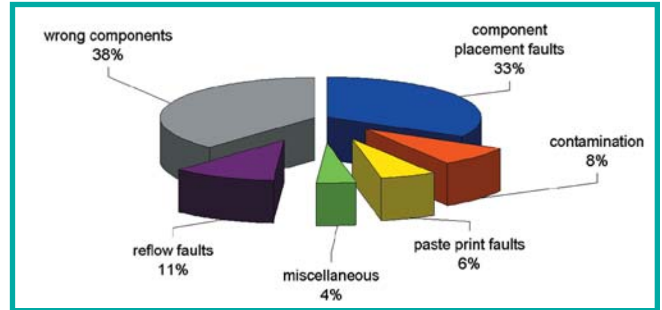

FIGURE 4: Fault distribution.

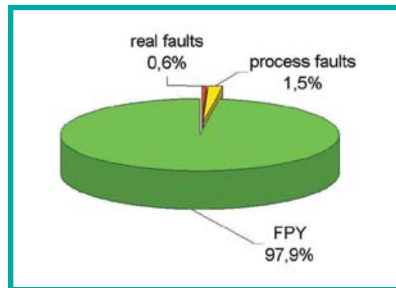

FIGURE 5: First pass yield, paste.

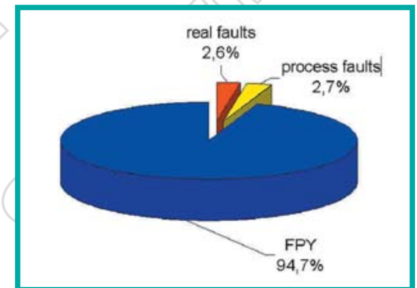

FIGURE 6: First pass yield, component in paste.

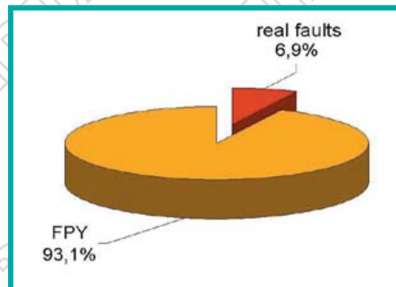

FIGURE 7: First pass yield, reflow.

Conclusion

Contrary to the common, frequently quoted assumption that paste faults represent the primary percentage or 70% of all faults in the printed circuit assembly process, this detailed analysis shows that those faults amounted to only 8.3%.

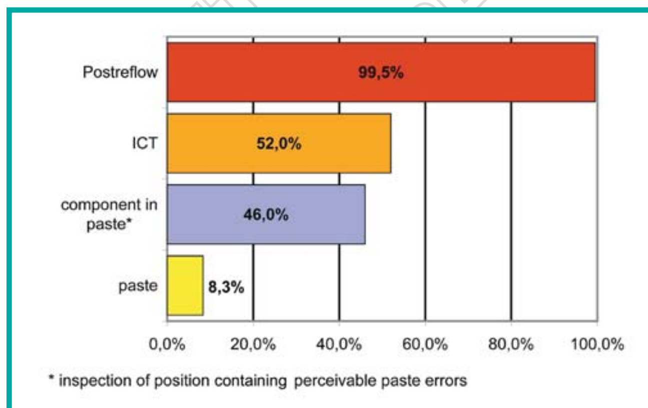

FIGURE 8: Fault coverage at different testing locations.

Forty-nine percent of the true faults were detectable only after soldering. These consisted of component and soldering faults. Forty-eight percent of the optically recognizable faults could not be recognized electrically. This result means that optical inspection is necessary.

This test showed that paste inspection and component inspection detect a relatively high percentage of process faults; here, it amounted to over 50%. These faults are, in fact, true faults; however, they correct themselves during the subsequent process steps. Paste or pre-reflow quality control is certainly practical for process optimization to avoid mass production faults or recognize faults in the production equipment. However, in the final analysis, the process faults are not relevant for the quality, and premature repair would be inefficient and cost intensive.

Even though this test setup cannot be generalized in all details, these comprehensive results do show that post-reflow AOI is a key factor in the production process and is very well suited for detecting relevant faults. ■

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