分析家们预测，微电子机械系统（MEMS）和微系统的市场规模将在2005年以前达到680亿美元。微系统技术和MEMS生产的服务、材料和设备供应商基础设施正在快速发展。最近几年，建立了很多铸造厂和设计所。但是，封装仍然是个问题，并常常拖延工业化和商品化进程。选择适当的封装方法可通向产品的成功之路或导致产品的夭折。因此，选择正确的技术对于成功的产品设计是必不可少的。

MEMS Packaging is Still a Challenge

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Opportunities exist, though, for innovative service providers.

Forecasters and analysts predict the market size for micro-electromechanical systems (MEMS) and microsystems to be $68 billion by the year 2005 (NEXUS Market Study 2002). The markets for nanotechnology are expected to far exceed microtechnology markets, if all technology areas—such as nanomaterials, nanocomposites, catalysts, coatings and nano-biotechnology—are considered. Most nanotechnology products will need microtechnologies at their interface to the real, macro world. Underpinning these staggering market expectations for micro-nanotechnologies (MNT) is an infrastructure of services, materials and equipment suppliers.

The infrastructure for microsystem technologies (MST)/MEMS development and production is growing fast. A large number of foundries and design houses have been established over the past few years that cover most, if not all, of the range of the required technologies for commercializing micro- and nanotechnology. Packaging, however, still remains a bottleneck, often introduced belatedly at the end of the design cycle where it can delay or even prevent industrialization and commercialization. Selecting the proper packaging method may tip the scales toward either a product's success or its premature failure. Choosing the right technology, therefore, is not a marginal concern but pivotal to the product design.[1]

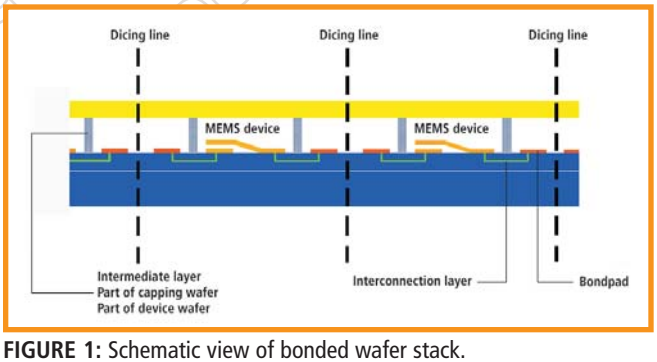

FIGURE 1: Schematic view of bonded wafer stack.

Packaging for MST/MEMS

Packaging and assembly for MST/MEMS are, in general, more costly than their equivalents for standard integrated circuits. This expense is, primarily, due to the diversity of the interconnections, which are multi-functional and may incorporate electrical, optical and fluidic. Also, the high levels of accuracy and the potential sensitivity of the devices to mechanical and external influences play a major role in the cost aspects of the final MNT product. A third aspect is the fragility and sensitivity of many devices, such as electrical and optical switches, micromirrors and membrane-based sensors.

For nearly all MST/MEMS products, packaging and assembly are the areas of full integration, where the electrical, mechanical, optical, fluidic, magnetic and other functions come together and where the problems associated with the concentration of such a diversity of functions present a major challenge to the designers. Conflicting demands, such as functionality vs. costs, and technical hurdles have to be overcome. In addition, MST/MEMS are by nature application-specific, and solutions are not always transferable from one product to another. This fact can lead to application-specific solutions, as opposed to generic

ones. The infrastructure for MST/MEMS is at the beginning of development, but designers can already benefit from experience gained by others in the field, especially from professional suppliers.

MST/MEMS are mostly associated with non-standard techniques, including processing and highly application-specific solutions, which in practice is not generally the case. Several examples of established packaging concepts can be used with some modifications for MST/MEMS.

	Temp. (°C)	Outgassing during life time	Creation of cavity	Loss of real estate	Strength of bond	Remarks
Anodic	300–500	No	No	Limited	Very good	Flat surface and high voltage needed
Silicon direct	>700	No	Yes	Limited	Very good	
Glass frit	400–650	No	Yes	Considerable	Medium	Small process window
Polymer	<200	Yes	Yes	Medium	Medium	
Eutectic	370–400	No	Yes	Medium	Medium	
Solder	250–350	No	Yes	Medium	Medium	
Direct	<100	No	No	Limited	Medium	Very flat surface and special surface treatment needed

TABLE 1: Advantages and disadvantages of various wafer bonding technologies.

Ceramic Packages for MST/MEMS

Ceramic packages are ideal when stress is a concern, as is the case with many MST/MEMS products. Following placing and fixation of the die in the package cavity, wire bonding ensures electrical interconnection and the cavity can, subsequently, be sealed by a lid. The lid can also be transparent for optical applications. Being so close to the packaging of standard products, this technology is offered by many companies. Some even run at relatively high volumes. An important advantage especially for MST/MEMS is that small volumes are possible without high setup cost.

Semi-Standard Packaging

For classic plastic chip packages, the chip is first mounted on a leadframe, and the wirebonder introduces the electrical interconnection from each bond pad to the pins on the leadframe. Finally, the entire construction is sealed with black thermoplastic.

At first plastic moulding processes were regarded as fundamentally unsuitable for MST/MEMS due to the processing conditions being too harsh for the often very fragile devices with their moving structures or sensitive sensor areas. In addition the need for other interconnections, such as optical or fluidic, or the need for hermetic—as in accelerometers—prevents the straightfor-

ward application of this technology. However, a number of manufacturers have found solutions for these problems.

One method is to cover the sensitive sensor area during moulding by a cap. That cap prevents fluid compound reaching the sensor area during filling of the moulding cavity. In this concept the whole die, including the gold wires, is covered by the moulding compound, which results in good mechanical protection and comparable reliability properties as with standard packages. Depending on the application, this opening can be covered by a lid.

The use of thermoplastic mould compounds with pre-plated leadframes is one of the most mature and low cost solutions for volume manufacturing. For low volumes, the tooling cost can be a big financial hurdle, which is especially true for MST/MEMS—a sum of niche markets each asking low volumes.

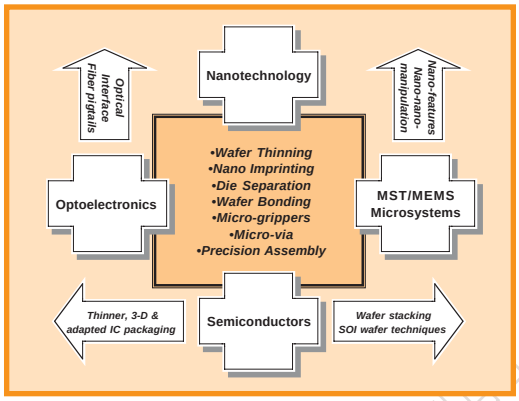

FIGURE 2: Driving forces on several processes used by MST/MEMS and other industries.

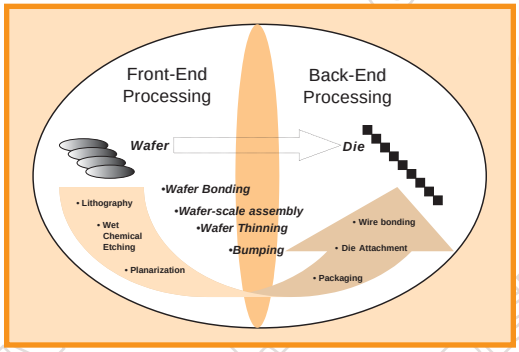

FIGURE 3: Processes crossing the borders between front end and back end processing.

Wafer-Scale Packaging

Wafer-level protection before assembly involves an extra wafer fab (or assembly) process. The wafer is covered by a cap, which protects the sensitive sensor area before the dicing process. Individual lids can be placed on top of each sensor or a second wafer with preformed cavities can be placed on top of the sensor wafer. This cavity can allow room for the micromachining structure to move (Figure 1). The second wafer can also have interconnections or other functionalities.

Typically, only two wafers are bonded, but for some applications even triple wafer constructions are used. Depending on the bonding technology used, the bond can be hermetic, providing a vacuum or gas-filled area and preventing contamination from entering. This construction makes the MST/MEMS device robust, but ensuring interconnection with the outer world is not always straightforward and the ensuing thickness of the devices can be a showstopper for applications where space is limited.

Wafer bonding needs a technology to ensure the adhesion of one wafer to the other. This bond must be able to withstand external forces and temperature changes during the rest of the assembly process and during its lifetime. This technology can use an intermediate layer, like solder, glass frit or polymer. Alternatively, the surface can be activated, and direct bonding can be used, strengthened by temperature or high voltage treatment. An overview of bonding pros and cons is given in Table 1.

In general bonding with an additional layer is advantageous when a cavity is wanted. The extra material to be added to the product can, however, lead to reliability problems or influence the performance of the device. Also, the area needed for the bonding material leads to loss of space for the devices. Most bonding technologies need large driving forces to create a strong bond, either by high temperatures or high voltages, which is unwanted and can harm the devices. Therefore, much interest has been generated in bonding at low temperatures. Several suppliers are now offering equipment and processes for this type of bonding. Accuracies from wafer to wafer are typically in the 10 micron area, although lower tolerances have been demonstrated. Accuracies are not only determined by alignment accuracies but also by limitations in alignment marks and thermal mismatches.

The mean advantage of wafer bonding lies in the fact that the sensitive and fragile sensor is protected during the packaging and assembly process. It is also attractive while the process is wafer-scale, which is potentially more cost effective as compared to die-scale processing. Electrical interconnection is a particular problem for wafer-scale packaging, as the bond pads are hidden by the capping wafer. One option is to provide access to them via the scribelines. Another option is to make electrical interconnections via through holes either in the capping wafer or in the sensor wafer. This process is more expensive, although it could lead to better use of real estate and, supplemented with a bumping process, to a flip chip mountable device.

Trends in High-Volume Electronics

Semiconductors have long been dominated by the large-volume products like microprocessors and memories. Product portfolios have become more diverse, and numbers per product have gone down. Also, the technologies used are becoming more diverse. With regard to equipment, MST/MEMS, semiconductor and other industries' developments are often exploring similar technology options (Figure 2).

Historically, front and back end processing were sharply divided, with wafer test and final inspection being the last steps in the front end process and dicing the first step in the back end process. The borderline is becoming vague (Figure 3) with the introduction of wafer bonding—a wafer-scale packaging technology—and the decreasing feature sizes in back end processing.

Whatever technology path is chosen, most will require expensive process equipment and capital infrastructure, as well as

highly qualified and experienced engineers for setting up the designs and process flows.

Conclusion

One of the biggest hurdles for the swift industrialization and commercialization of MST/MEMS products is the barrier to high-volume electronics manufacturing. This barrier is caused by the high startup costs and the relative inflexibility of the industry, which is used to high volumes and fixed roadmaps. However, the semiconductor industry is currently facing several technology and market trends that can be beneficial for the MST/MEMS industry.

Over the past decade, semiconductors and MST/MEMS processing techniques have drifted apart, although they are based on similar underlying processes. Customer-specific demands tend to rule, and the integrated circuit (IC) industry was initially neglecting this market segment. As a consequence the MST/MEMS businesses and companies were forced to develop their own processes and equipment. In our investigation of the markets for back end services, we noticed a tendency to return to the benefits of the semiconductor industry by making use of adapted standard processing.

Technologies described in this article are in principle generic and can, therefore, be used for more then one customer or in different applications. This fact is of interest to the many relatively small customers in MST/MEMS because they need reliable and cost effective processes for relatively low volumes. The only way to achieve that is to use generic processes that can be used with minor modifications for many customers and products.

To conclude, packaging and assembly techniques for MST/MEMS still need to advance to the levels of the technologies associated with those that have evolved for the electronics industry. Current techniques remain sub-optimal, although further developments and collaborations are happening worldwide in this important field. ■

Reference

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