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Wafer-Level Packaging Today

Thomas Goodman and Peter Elenius

WLP represents one of the most exciting and innovative frontiers in the packaging industry.

Wafer-level packaging (WLP) has enabled new advances in the miniaturization and cost reduction of portable products through its chip-size form factor and gang (wafer-level) processing. Devices such as EEPROMs, integrated passive devices (IPDs) and analog chips in WLP are now used extensively in mobile phones and other portable consumer products. In addition, WLP has been adopted for new classes of devices such as power MOSFETs to enable their use in miniaturized equipment.

A clear definition of WLP is key to understanding the trends and limitations in this packaging class. Many wafers are prepped in wafer form for assembly, either with solder bumps, gold bumps or a number of other established or emerging technologies. These bumped flip chip devices are then mounted either on package substrates for later connection to a system board—commonly denoted as flip chip in package (FCIP)—or directly to the system board—flip chip on board (FCOB)—without the use of an interposer. The key difference between these flip chip devices and a WLP is that special equipment and/or processes are required to mount these parts, either because of requirements for placement accuracy or additional processing such as underfilling to ensure reliability.

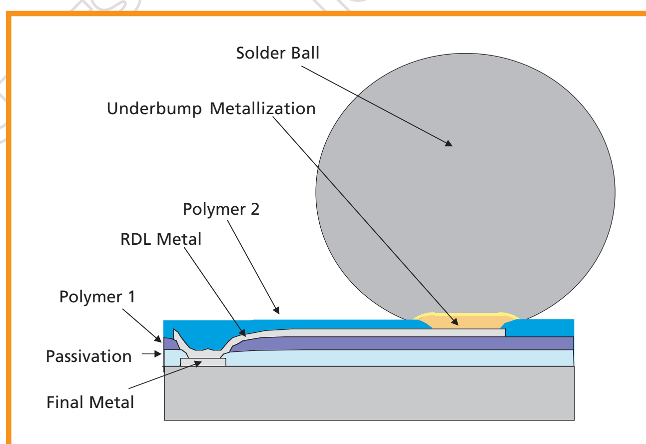

FIGURE 1: Thin-film type WLP.[1]

WLP, on the other hand, is a package that emerges from the dicing operation ready to be tested and assembled using conventional surface-mount techniques. Although the casual observer might think that a typical WLP with its larger solder bumps is just a flip chip on steroids, the requirements and technical challenges faced to make these packages manufacturable and cost-effective are demanding and unique.

History

That being said, the flip chip must be acknowledged as the granddaddy of WLP. Integrated device manufacturers (IDMs) started it all: IBM first introduced FCOB solder-bumped flip chip devices in its M360 mainframe in 1964, and Delco followed with solder-bumped devices for automotive in 1969. Japanese companies such as NEC and Hitachi began using FCOB devices in their mainframe and supercomputers in the 1970s. Plating- and solder paste-based processes became the basis for a number of merchant wafer bumping houses that were formed worldwide in the 1990s, such as Kulicke and Soffa's Flip Chip Division, Unitive, Fujitsu Tohoku Electronics and IC Interconnect. WLP technology was developed out of these companies' bumping and redistribution technologies; FCD's Ultra CSP® and Fujitsu's Super CSP were among the first WLPs to hit the market.

As the merchant bumpers began licensing their technology to the major packaging subcontractors starting in 1999, flip chip and these WLPs began to see widespread distribution to overseas manufacturing sites. For example, ASE (Taiwan), Amkor (Korea) and Siliconware (Taiwan) offer the Ultra CSP under license from FCD.

Package Types

As with any new package trend, a bewildering number of basic package structures and variations was initially offered; with time, reliability issues and manufacturability concerns have narrowed the field to a few key package types and manufacturers. The most widely manufactured

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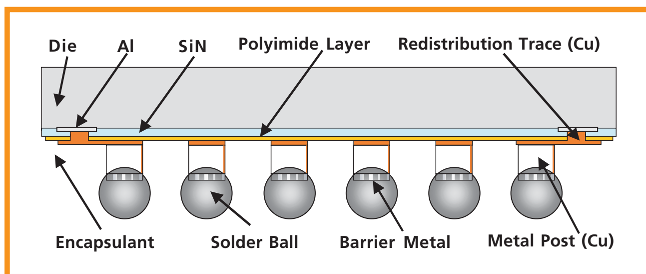

FIGURE 2: Cross-sectional view of copper-post-type WLP.[2]

type of WLP uses the thin-film, ball drop process employed by FCD, Unitive, IC Interconnect and others. Solder balls with diameters of 0.3 mm to 0.5 mm are placed and reflowed on sites prepared with under bump metallization (UBM). These packages can closely resemble a conventional solder-bumped flip chip die, but important manufacturing, design rule and structure differences make this process workable for large-pitch, large-solder ball applications. This type of thin-film package, produced by companies such as FCD (Ultra CSP), Unitive (Xtreme CSP™), IC Interconnect, Micron and others, is shown in Figure 1.

A structure in use by companies in Japan such as Casio, Fujitsu and Shinko makes use of a plated copper post at each ball site (Figure 2). These posts, which are typically on the order of 100 µm in height, are encapsulated in epoxy. The ends of the posts, which are exposed by using one of a couple of different processes, are plated as UBM and serve as sites for the attachment of large solder balls.

Other WLP structures brilliantly serve niche markets. One example is the ShellBGA from ShellCase in Israel. This package features optically clear glass substrates on either side of the die for protection. As such, it is used extensively for optical components such as CCDs and CMOS image sensors.

Drivers, Applications

WLPs as defined above are used predominantly for two reasons: for minimal form factor and for low cost. Because WLPs are processed in wafer form and then diced, they are true chip-size packages. This type of packaging is ideal, then, for portable applications; indeed, the majority of WLPs produced today are for mobile handsets, personal digital assistants (PDAs), portable computing and other wireless appliances.

WLP used in these cost-sensitive mobile consumer products are typically mounted on cost-effective, conventional printed circuit board (PCB) technology and, therefore, have generally been limited to gross pitches of 0.5 mm or greater. In addition, because WLPs are generally assembled using conventional surface-mount techniques that preclude the use of underfill, reliability requirements in the form of thermal cycle performance force a limitation on the size of the chip that can be packaged in WLP. Specifically, the limitation is the difference in the coefficients of thermal expansion (CTE) of the silicon and the medium upon which it is being mounted, typically an organic or ceramic laminate. Large chips see greater strain and, hence, stress during thermal cycling than do small ones, and, therefore, solder bump fatigue and failure occur more quickly. For this reason, the effective range of use for WLPs at 0.5 mm pitch is generally for devices with four to 36 I/O.

Still, WLPs have application in a variety of small, high-volume devices such as IPDs, EEPROMs and power MOSFETs.[3] One example is a power MOSFET packaged in a WLP from International Rectifier, shown in Figure 3. The wafers are bumped by IC Interconnect by dropping solder balls on an electroless nickel/gold UBM.

FIGURE 3: MOSFET in WLP from International Rectifier.

Another example of small die being packaged in WLP for small form factor applications is in the Handspring VisorEdge PDA, shown in Figure 4. The four IPDs used for electrostatic discharge (ESD) protection are mounted on the board along with other surface-mount components.

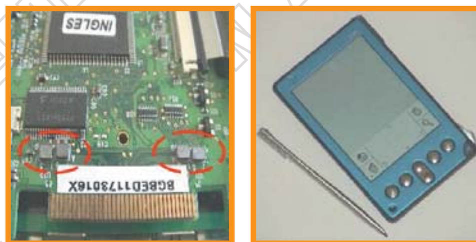

FIGURE 4: PDA designed with IPDs in WLP.

Casio packages more functional devices in WLP for use in its small form factor products such as watches and wrist cameras. Figure 5 shows the use of two WLPs in Casio's color data wrist camera. The devices shown in the picture are:

1. 109 I/O CPU, in 0.5 mm WLP
2. 48 I/O 8Mb flash, in 0.5 mm WLP
3. 48 I/O 2Mb SRAM, in land grid array (LGA).

Enablers for WLP

Several areas of WLP technology, if further developed, could significantly expand the applicability of the technology.

Bump Compliancy

Currently, the use of WLP is limited by the thermal cycle reliability of devices with large ball arrays. Several technologies are under development that may extend the size of a WLP array that can be utilized without underfill.

One technology developed by Kulicke and Soffa's Flip Chip Division uses a polymer reinforcement layer around the base of the bump. The use of this polymer collar limits the strain and

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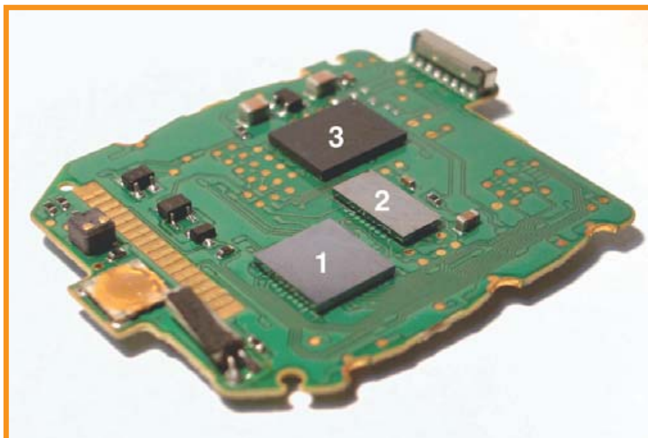
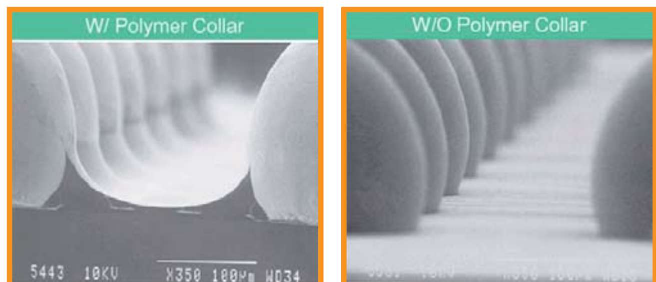


photo courtesy of Casio Computer

FIGURE 5: WLPs enabling a wristwatch with color camera.



photos courtesy of K&S Flip Chip Division

FIGURE 6: Cross sections of bumps with (left) and without (right) the polymer collar reinforcement.

stress on the solder bump, extending its fatigue life. Figure 6 shows cross sections of bumps with and without the polymer collar reinforcement. This structure has been shown to give a 64% increase in thermal cycle reliability and is accomplished on a 10 x 10 array of solder bumps on a 0.5 mm pitch.[4]

Wafer-Level Burn-In and Test

As low cost is one important driver for WLP, the development of wafer-level burn-in and test (WLBI/T) capability will be key to mass adoption of wafer-level packaging for a given device technology. Because of issues with power distribution, contact technology, CTE issues (aggravated by the move to 300 mm wafers) and cost, the WLBI/T may be limited to low I/O devices such as memory or micro-electromechanical systems (MEMS).[5] Certainly, the prospect of application of any technology to ultra high-volume products such as DRAM is enough to spur aggressive development.

Wafer Thinning

The primary basis of solder ball fatigue in thermal cycle testing and field use is the mismatch of CTE between the silicon and the substrate upon which it is mounted. Also related is the rigidity of each component; thinner die will be more flexible and, therefore, will extend the fatigue life of the solder balls. Thinning a wafer before the WLP process is risky as it increases the likelihood of breakage and warpage. Thinning after completion of WLP processing, including solder ball attach, is preferable but difficult. Technologies and equipment to successfully thin and stress-relieve wafers that have been processed as WLP are under development.

Wafer-Applied Reflowable (No Flow) Underfill

Underfill extends the fatigue life of solder ball arrays in flip chip devices. Underfill, however, does not fit into a low-cost surface-mount assembly process. If underfill could be applied at the wafer level during WLP processing, it would provide a potentially low cost solution for extending the application of WLP while maintaining ease of integration into standard surface-mount lines. Much work is underway to develop wafer-level underfills.[6]

PCB Design/Cost

Although companies in Japan are pushing the standard pitch for WLP from 0.5 mm to 0.4 mm and below, the cost of substrates still makes finer pitch WLP prohibitively expensive for most applications. The development of lower cost mounting substrates for 0.4 mm pitch WLPs would permit the design of smaller solder ball arrays with correspondingly higher fatigue lives.

Why Not WLP?

For every good technology, a score of others exists, all competing for a socket or a designer's share of mind, and WLP is no exception. The ultimate goal of using WLP is either reduction of form factor and/or cost, and other technologies fit the bill as well or better than WLP, depending on the application.

For example, flip chip BGAs (FCBGAs) are a very manufacturable option for low- to mid-pincount devices, albeit an expensive one. However, the technology is ubiquitous, the capacity is available and prices are coming down.

Stacked die packages commonly offer silicon efficiencies in the 200% to 300% range as compared with 100% for WLP, multi-function integration (ASIC, SRAM and flash together) and accessibility to low-cost, wire-bonded BGA manufacturing capacity worldwide. Several companies worldwide, including Intel, Sharp and Fujitsu, are shipping five-die stacked packages in production quantities. Intel alone has shipped more than 100 million stacked packages to the industry.

And do not forget conventional wire bonding: Wire-bonded CSPs and BGAs are plentiful, cheap and still small enough to fit the bill for many portable applications. For example, a teardown of one leading-edge 2.5G phone from Japan revealed only wire-bonded CSPs and BGAs to support its miniature size, color display, MP3 player and Internet capability—no cutting-edge package required!

Cost of WLP: The Conundrum

One important driver for the use of WLP, in addition to form factor, is low cost. Because WLPs are gang processed at the wafer level, low cost can be achieved if the die size is small and the I/O

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count per die is not large. A small die size is important as the cost of processing the wafer can be spread over a large number of die. A low I/O count is typical for devices in WLP, and it is critical as excessive use of solder balls can drive up the cost of WLP processing significantly.

Although cost is an important driver for the development and use of WLP, the industry continues to develop technologies to extend the application of WLP to larger and more functional die. The WLP Conundrum thus emerges: One can extend the application to large die but in doing so will lose WLP's economy of scale.

Accelerating the Proliferation of WLP

Like the enabling technologies listed in the previous section, development of the infrastructure to support WLP is key to proliferation of this type of packaging.

• **Intellectual property (IP) development and deployment:** Development of enabling technologies is important, but deployment of the technologies through licensing or other means is critical to widespread adoption.

• **Multiple merchant WLP foundries:** IDMs that will use WLP technology in high volume such as memory makers will bring in and practice the technology in-house. However, merchant WLP foundries are required for those companies that do not have the production volumes to justify capital investment for in-house manufacturing. In addition, both companies using WLP foundries and IDMs practicing the technology in-house will have to have competent second sources for their WLP processing.

• **Regional service:** The logistics of moving a wafer from its point of fabrication to the WLP line to the test line will determine the optimum location for WLP processing. Not only are multiple WLP foundries required, they must be conveniently located near IDMs and wafer foundries worldwide to permit efficient flow of devices from wafer fab through test and ship.

• **Standards:** Standards for WLP structure and technology will allow for decreased time-to-market and help to eliminate the need for requalification when switching or second-sourcing a different WLP foundry.

Summary

WLP technology is an established, growing area of packaging that is being driven by the need for lower cost and/or form factor reduction. Principally, WLP is being applied to small, low I/O count die, although new technology is available that incrementally extends the use of WLP to larger die. New technologies and lower cost are required to expand the application to large, high-volume die such as DRAM or finer pitch solder ball arrays.

Finally, each application will use the most cost-effective package that it can to satisfy the required design. Because of the technology alternatives to using WLP available, WLP needs to grow as a technology and become an enabler of products in the future to become pervasive. ■

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Thomas Goodman *(email: tgoodman@egtechpartners.com) and* ***Peter Elenius*** *are with E&G Technology Partners, LLC, Tempe, AZ.*

A version of this article was originally published in the 2003 SMTA Pan Pacific Microelectronics Symposium Proceedings.

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