



Do you like news and articles like this?

Then, get it from the **ORIGINAL** source ... [PCB UPdate](#) ...
the semi-monthly e-mail newsletter produced by **Circuits Assembly**
and **PCD&M** and circulated to over 40,000 readers.

[CLICK HERE TO READ THE ARTICLE YOU REQUESTED](#)

Optimizing Solder Paste for Wafer Bumping

Maureen Brown and Fritz Byle

This investigation examines the variables of wafer bumping using solder paste printing techniques.

Solder paste is used for an array of electronics assembly applications and is finding more uses for the microelectronic and semiconductor industry. Wafer or substrate bumping, which is creating bumps or interconnects on wafers and substrates with very fine mesh solder pastes, has created much interest.

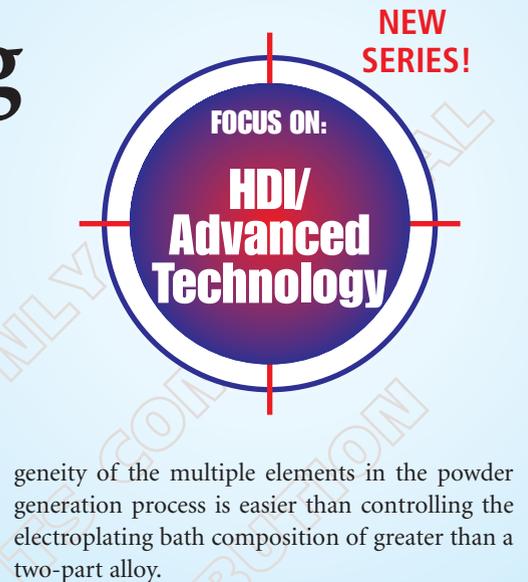
Several options for bumping a wafer are currently in use. Solder paste printing is the second most common method, with electrodeposition, gold stud bumping, evaporation and ball placement in the minority.¹ Electroplating is a popular bumping technology that drives tighter pitches capability. After the under-bump metalization (UBM) is deposited onto the wafer, a photo resist is applied, exposed and developed. The solder is selectively plated as the UBM acts as an electrode for the plating process. The photoresist is then removed, and the wafer undergoes a reflow process to form spherical bumps.⁷

The solder paste bumping process typically places the wafer in a fixture for additional support during the stencil printing process. An automated measurement system in-line that quantifies the volume of solder paste deposited for process monitoring is beneficial. The bumps are then formed in an inerted reflow oven. For later processes the wafer must be cleaned to remove any flux residues. The bumps are subsequently inspected to ensure coplanarity.

The main driver for solder paste bumping gaining in popularity is its lower costs as compared to other bumping technologies.¹¹ On average the cost of electroplating is 2.2 times greater than solder paste bumping.⁵

Lead Free

Due to recent lead-free elimination policies worldwide, solder paste bumping should be capable for a large range of lead-free alloys (binary, ternary and quaternary). Solder paste bumping will inherently be an easier drop-in solution than plating technologies, as maintaining the homo-



geneity of the multiple elements in the powder generation process is easier than controlling the electroplating bath composition of greater than a two-part alloy.

Voiding

Another major concern of solder paste bumping is the presence of voids as compared to electroplating. The current upper specification limit promoted by electroplating service providers is 10% voids. As solder paste has evolved over the last several years, the voiding levels have declined. In most applications solder paste bumping void levels are competitive to the electroplating process, and in some applications voiding can be reduced to levels below 3 to 5%.

Technology Limitations

The current greatest limitation of the solder paste bumping process is the minimum pitch, which is 180 to 200 microns. This limitation has been challenged by the marriage of a photoresist as an in-situ stencil that creates a cavity, which facilitates the low cost processing of solder paste bumping. This innovative intermingling of the best of the two most common wafer bumping technologies allows this lower cost option to print to tighter pitches as low as 70 to 100 microns.^{2,3,8}

Solder paste suppliers are investigating finer solder powders to further permit solder paste bumping of tighter and tighter pitches. The current demand is for Type 5 powder with greater interest for Type 6. Very few applications require finer particle size distributions than Type 5 or 6, but suppliers of wafer bumping pastes are anticipating future industry demands and development work is continuing.

The further improvement for a capable process has been largely driven by the forecasted demands of the industry. Flip chip (FC) applications are growing.¹⁰ Prismark Partners reported a compounded annual growth rate (CAGR) of global FC production from 2000 to 2005 at 45% annually.^{4,5} Beyond the increasing demand of FC opportunities, the industry trend wants to increase the I/O count with an emphasis of maintaining die footprint area. Decreasing the pitch is the most common method to meet market demand of increased I/O count.

Project Setup

This overall project was designed to focus on the various key process modules that affect the final yield for a wafer bumping production line: printing, reflow and cleaning. This article reports on the initial phase where the greatest majority (>60%) of yield loss might be attributable to the printing module. The stencil layout attempted to take into consideration the current state of the market and the future demands of aperture dimensions and pitch.

An electroformed stencil with electropolished and nickel-plated aperture sidewalls was utilized for the experiments. Stencil thickness was 50 micron, and the aperture shape was square with corner radius. The aperture dimensions and the area ratios for the 10 varying dimensions and four different pitches are tabulated in Table 1. This stencil was used to assess the transfer efficiency, stencil aperture blockage rate and brick definition of the solder paste deposits.¹² Specifics are summarized in Table 1.

Solder Paste Materials

Substrate and wafer bumping applications require complete removal of the residues post-reflow. For paste bumping the flux residues must be completely and easily removed; therefore, water-soluble or aqueous chemistries were used in this experiment. The flux chemistries in this study differed in raw materials, viscosity

Area Ratio	Aperture Dimension (D)*	1.5D	1.75D	2D	4D
3.00	66	100	116	132	264
2.75	73	110	128	146	292
2.50	80	120	140	160	320
2.25	89	134	156	178	356
2.00	100	150	175	200	400
1.75	114	171	200	228	456
1.50	133	200	233	266	532
1.25	160	240	280	320	640
1.00	200	300	350	400	800
0.75	267	401	467	534	1068

*Note: The apertures are square geometries with a length and width of D (µm).

TABLE 1: Stencil apertures and pitches (all dimensions reported in µm).

	Paste A	Paste D
Chemistry	Aqueous	Aqueous
Viscosity	Low	Moderate
Tack	Low	Moderate
Metals %		
Type 5	90.0%	90.0%
Type 6	89.5%	89.5%
Type 7	88.0%	88.0%

TABLE 2: Solder paste property table.

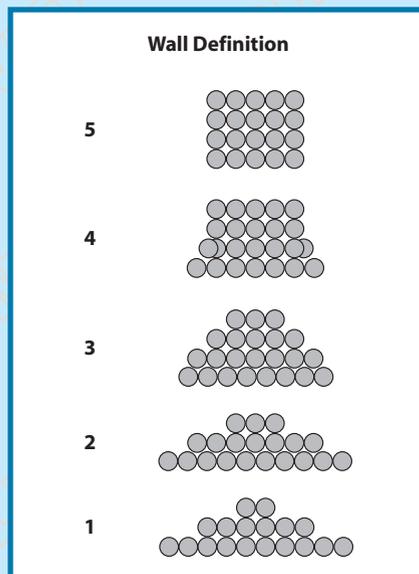


FIGURE 1: Solder deposit definition gauge.

and tack (Table 2). Differing viscosities and differing mesh sizes were used for applications ranging from utilizing a metal foil stencil for wafer and substrate bumping, along with those applications that have the stencil in place during the reflow.⁹

Procedure

A stencil printer with full platen support was used. The solder paste samples

were printed at a relatively low speed, less than 1 in./sec. on-contact printing, and the print pressure was optimized for each solder paste sample by concluding the optimal separation speed, squeegee pressure and print speed for each flux type. This phase of the experiment focused on the printing aspect, and, therefore, a planar non-solderable test vehicle was used. Several boards were printed for each solder paste sample.

The transfer efficiency rate, or, conversely, blockage of the apertures, and solder deposit definition were recorded for each sample.

Data Analysis

Three aspects were graded for this printing investigation: transfer efficiency of the stencil, blockage of the apertures and the solder deposition definition. The transfer efficiency was visually gauged based on the quantity of solder paste that was deposited on the test vehicle substrate. The solder paste blockage of the stencil defined the percent of apertures of a specific pattern post-printing that exhibited solder paste remaining in the apertures that would prevent acceptable paste release from the stencil. For each aperture dimension and pitch, 25 by 25 apertures were in a full area pattern. Lastly, the brick definition of the solder deposit was rated (Figure 1).

As seen in Tables 3 and 4, the area ratio had the greatest effect on the overall print quality and capability. The flux formulation chosen for the bumping process had a greater effect for complete paste release from the stencil (Table 5), while the powder mesh size had a greater effect on the quality of the brick definition (Table 6). From the data analysis the pitch had no significant effect on the solder paste release from the stencil or the definition of the solder paste deposit.

The flux formulation used in bumping applications did have an effect on reducing the clogging of the stencil apertures to maximum the transfer of solder paste (Table 7). Poor transfer of the solder paste

will ultimately impact the bump heights.

The aperture dimensions and stencil thickness had a significant effect on the rate of clogging the stencil apertures. Area ratios less than 1.25 are statistically equivalent with respect to the solder paste release potential. When the area ratio ranges from 1.5 to 2.0, the release of the solder paste reduces and the area ratios are significantly different (Table 8).

Tables 9 and 10 show that a significant difference did not exist between the Type 5 and 6 powder distribution to the clogging of the stencil apertures. The finer powder distribution had a greater release characteristic to the coarser powders, but the finer powder mesh sizes of Type 6 and 7 have statistically superior brick definition to the coarser Type 5 distribution. The powder size distribution should not be selected based solely on the successful release potential or the wall definition, as the finer particle size distributions have a greater surface area to mass ratio (SAM).

Analyzing the viscosity effect on blockage (Table 11), the lower viscosity (A-T7) samples improved the deposit definition and transfer efficiency as compared to those solder paste samples that had higher viscosity (D-T5). The samples of the highest viscosity were greater than twice the lowest viscosity sample to study a wide range. Based on this experimentation, viscosity was not statistically significant for the 0.75 area ratio test pattern only (F ratio = 6.7). With other area ratios such as 1.75,

Source	Nparm	DF	Sum of Squares	F Ratio	Prob > F
Area Ratio	9	9	408651.27	1668.26	<0.0001
Flux	1	1	504.60	18.5396	<0.0001
Mesh	2	2	555.60	10.2067	<0.0001
Pitch	1	1	0.00	0.0000	1.0000

TABLE 3: Effects test on blockage.

Source	Nparm	DF	Sum of Squares	F Ratio	Prob > F
Area Ratio	9	9	576.78483	722.7974	<0.0001
Mesh	2	2	31.69527	178.7351	<0.0001
Flux	1	1	0.65104	7.3427	0.0072
Pitch	1	1	0.03841	0.4332	0.5111

TABLE 4: Effects test on brick definition.

Flux Level	Least Sq Mean
D A	57.600000
A B	54.700000
Levels not connected by same letter are significantly different.	

TABLE 5: Flux effect on blockage.

Flux Level	Least Sq Mean
A A	2.4450000
D B	2.3408333
Levels not connected by same letter are significantly different.	

TABLE 6: Flux effect on brick definition.

the viscosity of the material, though, did have a statistically significant effect (F ratio = 30.5). Therefore, as the print deposit decreases in relation to the surface area of the aperture walls, the viscosity of the solder paste needs to optimize for the challenging application requirements.

Discussion

Measurement Issues

In evaluating the printing results, a visual approach was necessary due to the difficulty encountered in locating repeatable, automated inspection equip-

ment for quantifying the volume of the solder paste deposits. The majority of available inspection tools are geared for post-reflow bump inspection or for paste deposits on a surface-mount scale (length and width dimensions >300 μm). The bumping application represents an extreme challenge for inspection equipment. For ±5% accuracy on 66 μm (0.0002 mm³) deposits, the equipment would need a resolution of better than 1 μm in x, y and z. This is coupled with the challenge represented by the specular wafer surface, though the extreme planarity is a benefit.

Verifying that the extremely low print defect rates needed for high-yield bumping processes are actually being achieved requires an exceptionally high statistical sample size. This requires that the measurement equipment be capable of accepting computer-aided design (CAD) input, as generating a program manually would be impractical. Though quantitative data collection is preferred, visual examinations are beneficial because one can easily and rapidly detect an isolated print defect in a closely spaced array of deposits.

Paste Technology Impact

The particle size distributions for Types 5 and finer are not yet well standardized. Therefore, the paste manufacturer and user should agree upon which of the manufacturer's powder types are appropriate in a given application.

Referring to Table 9, no statistical difference in blockage occurred between the Type 5 and the finer Type 6 distribution. This result was due to the large overlap in the Type 5 and Type 6 distributions. The current market demand has gravitated towards Type 6, as it fits the aperture sizes normally required for bumping and is typically more available than Type 5. Type 7 powder is normally only required for bumping extremely small apertures.

Another consideration regarding powder distribution to make an informed

Area Ratio Level	Least Sq Mean
2.75 A	100.00000
3 A	100.00000
2.5 A B	97.50000
2.25 B	95.16667
2 C	75.83333
1.75 D	51.50000
1.5 E	39.83333
1.25 F	1.66667
0.75 F	0.00000
1 F	0.00000
Levels not connected by same letter are significantly different.	

TABLE 7: Area ratio effect on blockage.

Area Ratio Level	Least Sq Mean
0.75 A	4.5812500
1 B	4.1250000
1.25 C	3.8750000
1.5 D	3.5729167
1.75 E	2.9583333
2 F	2.0000000
2.25 G	1.4166667
2.5 H	0.6958333
2.75 I	0.4458333
3 J	0.2583333
Levels not connected by same letter are significantly different.	

TABLE 8: Area ratio effect on brick definition.

Continued on pg. 56

Continued from pg. 25

mesh size selection is that the surface area to mass ratio (SAM), expressed in units of m^2/gram , varies inversely with the square of the particle size. In other words, halving the particle size increases the area per unit mass by a factor of four, assuming that the particle size distribution shapes are similar. This assumption is violated for small powders, as they often contain many fines, which raise the surface area even further. The amount of solder surface area in contact with the acidic flux vehicle that is designed to reduce metal and solder oxides is directly related to the difficulty of maintaining adequate shelf life and viscosity stability of the paste.

Conclusions

Paste bumping is a viable, capable and low cost technology for most of today's moderate and large pitches such as wafer-level packages (WLP) and many FCs. Automated process monitoring via volumetric data collection is an area of great opportunity to further facilitate this low cost bumping technology.

The flux chemistry as it impacts the rheology has a significant effect on the ability to release completely from the stencil as well as the deposit definition. The test results state that lower viscosity materials have improved release properties in comparison to higher viscosity paste. However, an inverse relationship to the deposit definition exists. Also from this testing, Type 6 distribution has proven to be a reliable defacto starting point for most bumping applications. The widely varying bumping application requirements demand close collaboration between suppliers and users to achieve the high yielding, low cost production of which paste bumping is capable. ■

References

1. Chip Scale Review, July 2002
2. Patterson, Deborah S., "Solder Bumping Step By Step," Advanced Packaging, July 2001.
3. Patterson, Deborah S., "Continued Improvements in the Use of Alloys and Polymers Enhance Wafer-Level IC Performance," Chip Scale Review, October 2002.
4. Prismark Partners, 2000, Cold Spring Harbor, N.Y.

Mesh Level		Least Sq Mean
6	A	57.300000
5	A	57.150000
7	B	54.000000
Levels not connected by same letter are significantly different.		

TABLE 9: Powder mesh effect on blockage.

Mesh Level		Least Sq Mean
7	A	2.7425000
6	A	2.5443750
5	B	1.8918750
Levels not connected by same letter are significantly different.		

TABLE 10: Powder mesh effect on wall definition.

Flux/Mesh Level			Least Sq Mean	
D-T5	A		58.800000	
D-T6	A	B	58.000000	
A-T6	A	B	C	56.600000
D-T7		B	C	56.000000
A-T5			C	55.500000
A-T7			D	52.000000
Note: Levels not connected by same letter are significantly different.				

TABLE 11: Viscosity effect on blockage.

5. Prismark Partners, 2001, Cold Spring Harbor, N.Y.
6. Prismark Partners, 2002, Cold Spring Harbor, N.Y.
7. Seiller, Jacky, "Bumping Technology," Advanced Packaging, April 2001.
8. Thompson, Terrence E., "Wafer Bumping: As the Technology Moves into the Mainstream, Some Technical Issues Remain," Chip Scale Review, July 2002.
9. Hamano, Toshio and Alex Papalexis, "Wafer Bumping Solutions: Consumer to Advanced Application," Advanced Packaging, October 2002.
10. Vardaman, E. Jan, "Growing Demand for Flip Chip," Advancing Microelectronics, Volume 20 Number 1, January/February 2003.
11. Huang, Dr. Benlih, Dr. Xiaohua Bao and Dr. Ning-Cheng Lee, "Low Cost Solder Bumping Via Paste Reflow," SMTA International 2001.
12. Schake, Jeffrey D., "Stencil Printing for Wafer Bumping," Semiconductor International, October 2000.0

Acknowledgments

The authors would like to thank Kester's Advanced Products Application Lab, Jeff Schake at DEK-USA and Bill Coleman and Dave Britton at PhotoStencil.

Maureen Brown is advanced products engineer; email: mbrown@kester.com; and Fritz Byle is senior advanced products engineer; email: fbyle@kester.com—both with Northrop Grumman, Kester, Des Plaines, IL.

A version of this article was originally presented at APEX 2003.